



POSTAL BOOK PACKAGE 2026

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COMPUTER SCIENCE & IT

Objective Practice Sets

Computer Organization & Architecture

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Basics of Computer Design

Multiple Choice Questions & NAT Questions

- Q.1** The computer performs all mathematical and logical operations inside its
 (a) Memory unit (b) Central processing unit
 (c) Output unit (d) Visual display unit

- Q.2** Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I

- A. Pointer
 B. Position Independent code
 C. Constant operand

List-II

1. Indirect AM
 2. Immediate AM
 3. Relative AM

Code:

A B C

- (a) 1 2 3
 (b) 3 2 1
 (c) 1 3 2
 (d) 2 3 1

- Q.3** The most appropriate matching of the following pairs is

Column 1	Column 2
X: Indirect addressing	1. Loops
Y: Immediate addressing	2. Pointers
Z: Auto-decrement address	3. Constant

- (a) X-2, Y-3, Z-1 (b) X-3, Y-2, Z-1
 (c) X-1, Y-3, Z-2 (d) X-3, Y-1, Z-2

- Q.4** Consider the following I/O instruction format for IBM 370 I/O channel

Operation Code	Channel Address	Device Address
----------------	-----------------	----------------

Then operation code specifies

1. Test I/O
 2. Test channel

3. Store channel identification

4. Halt device

- (a) Only 1 and 4 (b) Only 2 and 3
 (c) 1, 2, 3 and 4 (d) Only 1, 3 and 4

- Q.5** An interrupt that can be temporarily ignored by the counter is known as

- (a) Vectored interrupt
 (b) Non-maskable interrupt
 (c) Maskable interrupt
 (d) Low priority interrupt

- Q.6** A processor can support a maximum memory of 4 GB where memory is word addressable and word is 2 bytes. What will be the size of the address bus of the processor?

- (a) At least 2 bytes (b) At least 28 bits
 (c) At least 31 bits (d) Minimum 4 bytes

- Q.7** A digital computer has memory unit with 24 bits word. The instruction set consists of 150 different operations. All instructions have an operation code part and an address part. Each instruction is stored in one word of memory. How many bits are needed for the OP CODE and how many bits are left for the address of the instruction.

- (a) 8, 16 (b) 16, 64
 (c) 4, 8 (d) 8, 64

- Q.8** An instruction is stored at location 300 with its address field. At location 301 the address field has value 400. A processor register R1 contains the number 200. Evaluate the effective address matching the following addressing modes to their respective addresses.

A. Direct	1. 702
B. Immediate	2. 200
C. Relative	3. 400
D. Register indirect	4. 600
E. Index (R1 is index)	5. 301

- (a) A3 B5 D2 E4 C1 (b) A3 B4 C1 D1 E5
 (c) A5 B3 C2 D1 E4 (d) A4 B3 C1 D5 E2

Q.9 What is the most appropriate match for the items in the first column with the items in the second column:

Column 1:

- X. Indirect addressing
- Y. Indexed addressing
- Z. Base register addressing

Column 2:

- 1. Array implementation
 - 2. Writing relocatable code
 - 3. Passing array as parameter
- (a) X-3, Y-1, Z-2 (b) X-2, Y-3, Z-1
(c) X-3, Y-2, Z-1 (d) X-1, Y-3, Z-2

Q.10 In which of the following address mode, the content of the program counter is added to the address part of the instruction to get the effective address?

(a) Indexed addressing mode
(b) Implied addressing mode
(c) Relative addressing mode
(d) Register addressing mode

Q.11 Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I

- A. Stack overflow
- B. Supervisor call
- C. Invalid opcode
- D. Timer

List-II

- 1. Software interrupt
- 2. Internal interrupt
- 3. External interrupt
- 4. Machine check interrupt

Codes:

- | | A | B | C | D |
|-----|---|---|---|---|
| (a) | 2 | 3 | 4 | 1 |
| (b) | 2 | 1 | 2 | 3 |
| (c) | 3 | 1 | 2 | 4 |
| (d) | 3 | 1 | 4 | 2 |

Q.12 In a certain processor, a 2 byte Jump instruction is encountered at memory address 3010H, the Jump instruction is in PC relative mode. The instruction is **JMP - 7** where - 7 is signed byte. Determine the Branch Target Address

(a) 300B H (b) 3009 H
(c) 3003 H (d) 3007 H

Q.13 Processor XYZ supports only the immediate and the direct addressing modes. Which of the following programming language data structures cannot be implemented on this processors?

- 1. Pointers
 - 2. Arrays
 - 3. Records
- (a) 1, 2 and 3 (b) 2 and 3
(c) 1 and 2 (d) Only 1

Q.14 Word 20 contains 40
Word 30 contains 50
Word 40 contains 60
Word 50 contains 70

Which of the following instructions loads 60 into the accumulator?

(a) Load immediate 20
(b) Load direct 30
(c) Load indirect 20
(d) Load indirect 30

Q.15 Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I

- A. $A[1] = B[J];$
- B. $\text{while } [*A++];$
- C. $\text{int temp} = *x;$

List-II

- 1. Indirect addressing
- 2. Indexed addressing
- 3. Auto increment

Codes:

- | | A | B | C |
|-----|---|---|---|
| (a) | 3 | 2 | 1 |
| (b) | 1 | 3 | 2 |
| (c) | 2 | 3 | 1 |
| (d) | 1 | 2 | 3 |

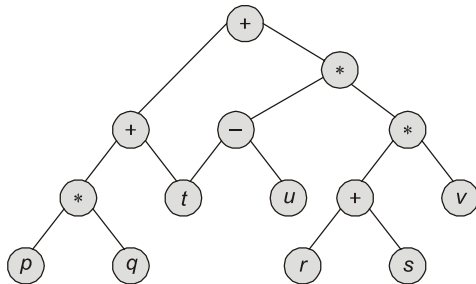
Q.16 In immediate addressing mode, where is the operand placed?

(a) In memory
(b) In stack
(c) In CPU register
(d) In instruction after opcode

Q.17 If the last operand performed on a computer with an 8-bit word has an addition in which the two operands were 00000010 and 00000011, what would be value of the overflow, sign and half-carry flags respectively?

(a) 0, 1, 0 (b) 0, 1, 1
(c) 1, 0, 1 (d) 0, 0, 0

in memory. The binary operators used in the tree can be evaluated by the machine only when all operands are in register. The instruction produce result only in a register.



What is the minimum number of registers needed to evaluate the expression if, no intermediate results can be stored in memory?

- (a) 3 (b) 4
(c) 5 (d) 6

■■■■

Answers Basics of Computer Design

1. (b) 2. (c) 3. (a) 4. (c) 5. (c) 6. (c) 7. (a) 8. (a) 9. (a)
10. (c) 11. (b) 12. (a) 13. (c) 14. (c) 15. (c) 16. (d) 17. (d) 18. (369)
19. (16383) 20. (b) 21. (b) 22. (d) 23. (c) 24. (b) 25. (b) 26. (3009) 27. (d)
28. (d) 29. (b) 30. (c) 31. (62) 32. (c) 33. (d) 34. (d) 35. (b) 36. (c)
37. (b) 38. (c) 39. (d) 40. (b) 41. (c) 42. (b) 43. (c) 44. (d) 45. (d)
46. (c) 47. (c) 48. (a) 49. (a) 50. (c) 51. (a) 52. (c) 53. (b) 54. (a)
55. (-128) 56. (a) 57. (a) 58. (b) 59. (d) 60. (a) 61. (d) 62. (16) 63. (d)
64. (b) 65. (c) 66. (a) 67. (d) 68. (92) 69. (2032) 70. (c) 71. (a) 72. (b)
73. (c) 74. (b) 75. (c) 76. (2048) 77. (d) 78. (a, b, d) 79. (c) 80. (b, c)
81. (a, c) 82. (b, c) 83. (b)

Explanations Basics of Computer Design

2. (c)

For making use of pointer in programs, indirect addressing mode is used.

Pointer stores the address of a variable and indirect addressing mode stores address of effective address the instruction.

Position independent code make use of relocation concept which is implemented by the use of relative addressing mode which uses relocation register to set the difference of logical and physical address.

Immediate addressing mode provides the value directly in the instruction which is suitable to be used for constant operands of the program.

4. (c)

The operation code specifies one of eight input output instructions: Start input/output, start input/output fast release, test input/output, clear input/output, halt input/output, halt device, test channel and store channel identification.

5. (c)

Maskable interrupt temporally ignored by counter.

6. (c)

$$\text{Memory size} = 4 \text{ GB} = 2^{32} \text{ B}$$

$$\text{Word size} = 2 \text{ B}$$

$$\text{So, unique address} = \frac{2^{32}}{2^1} = 2^{31}$$

Hence, atleast 31 bits are required.

7. (a)

Each instruction is stored in one word of memory.
Memory is word addressable and 1 word = 24 bits
 \Rightarrow 3 bytes.

Total number bits = 24

The instruction set consists of 150 different operations. To generate 150 different operations we need minimum 8 bits are required.

OP code	Address
8	16

So, option (a) is correct.

8. (a)

For direct, EA = address field value in IR (instruction register) = 400

For immediate, actually no meaning of effective address. So, EA here will be just the address of the operand field which is otherwise address field = 301.

For relative addressing, we have EA = PC value (current) + Address field value

$$EA = 302 + 400 = 702$$

For register indirect, the EA is the content of the register, the register name being present in the address field of instruction.

So, EA = content of R1 = 200

For indexed mode = Base address + index register content

$$= 400 + 200 = 600$$

So, option (a) is correct.

10. (c)

In relative addressing mode content of the program counter is added to the address part of the instruction to get the effective address.

So, option (c) is correct.

11. (b)

- Stack over flow is a internal interrupt.
- Supervisor call is a software interrupt.
- Invalid opcode is a internal interrupt.
- Timer is a external interrupt.

12. (a)

The Jump instruction is at address 3010 H and instruction is 2 bytes. Therefore, PC points to 3012 H on execution of this instruction.

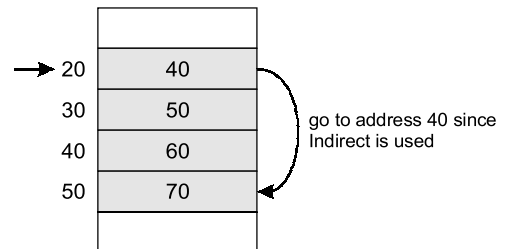
$$\begin{aligned} \text{Now Branch Target PC} &= \text{PC} + (-7) \\ &= 3012 \text{ H} - 7 \text{ H} = 300 \text{ BH} \end{aligned}$$

14. (c)

The given information can be understood as

20	40
30	50
40	60
50	70

Now load indirect 20 will load 60 into as follows



Hence (c) is correct option.

16. (d)

In immediate addressing mode, the operand is specified in the instruction itself.

For example: MOV R1, 12H is the immediate AM with 12 is operand.

17. (d)

$$\begin{array}{r} 00000010 \\ 00000011 \\ \hline 00000101 \end{array}$$

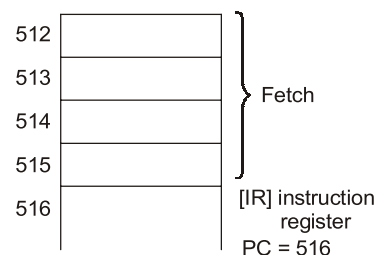
Overflow = 0, sign = 0, half carry = 0

Half carry indicate addition of pack at decimal numbers. When carry takes out of the lower digit order, this flag is set.

Auxiliary carry is also known as half carry.

18. (369)

4 byte instruction storage



Effective address = PC + Relative value

$$\text{Relative value} = \text{EA} - \text{PC}$$

$$= 885 - 516 = (369)_{10}$$

So, answer is 369.

19. (16383)

(6)	(6)	(6)	
Opcode	R_1	R_2	Immediate

$32 - (6 + 6 + 6) = 14$ bits for immediate field
 $\Rightarrow 2^{14} - 1 = 16383$ maximum possible value of immediate operand.

20. (b)

MDR register needed to read or written data into or onto memory location.

21. (b)

Four address instruction format:

Opcode	A_1	A_2	A_3	A_4
8 bits	24 bits	24 bits	24 bits	24 bits

So total bits needed = $(24 \text{ bits} \times 4) + 8 \text{ bits}$
 $= 96 + 8 \text{ bits} = 104 \text{ bits}$

So number of bytes = $\frac{104}{8} \text{ byte} = 13 \text{ bytes}$

22. (d)

$M[1000] = 18$, $M[1001] = 1$, $M[1020] = 16$

MOV I R_S , 1 $R_S \leftarrow 1$
 LOAD R_D , 1000 (R_S) $R_D \leftarrow M[1000 + [R_S]]$
 $R_D \leftarrow M[1000 + 1] = M[1001]$
 $R_D \leftarrow 1$
 ADD I R_d , 1000 $R_d \leftarrow R_d + 1000 = 1 + 1000 = 1001$
 STORE I 0(R_d), 20 $M[0 + R_d] = 20$
 $M[R_d] = 20$
 $M[1001] = 20$

23. (c)

As the instruction are 24 bit or 3 bytes, the value of program counter at any time should be multiple of 3 starting from 300 like 300, 303, 306 ... from options, '600' is multiple of 3 or is included in above series.

24. (b)

RTL $R_0 \leftarrow R_0 + R_1$
 The sequence of microinstruction take place in following cycles.

I cycle: $R_{1 \text{ out}}, S_{\text{in}}$

II cycle: $R_{2 \text{ out}}, T_{\text{in}}$

III cycle: $S_{\text{out}}, T_{\text{out}}, ALU_{\text{add}}, R_{\text{in}}$

3 cycles will be required to execute.

25. (b)

RTL $R_n = PC + 1$
 $P_c = M[PC]$

The sequence of microinstruction take place in following cycles.

I cycle: $PC_{\text{out}}, S_{\text{in}}, MAR_{\text{in}}$ (MAR can be loaded with PC_{out})

II cycle: $S_{\text{out}}, ALU_{\text{increment}}, R_{n \text{ in}}$

III cycle: $MDR_{\text{out}}, PC_{\text{in}}$ (MDR_{out} can be performed once MAR_{in} has been performed)

\therefore 3 cycles will be required to execute.

26. (3009)

Word addressable storage

3000 – 3001

3002

3003

3004

3005

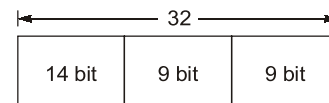
3006

3007-3008

3009

Valid program counter value after program is 3009.

27. (d)



2^{14} two address instructions are possible. Here, 400 two addresses are needed.

So, $(2^{14} - 400)$ opcode are free.

We can store $(2^{14} - 400) \times 2^9$ one address instructions.

28. (d)

Index addressing mode:

Effective address = [Base address + Displacement]

29. (b)

CPU clock cycles = $\sum CPI \times c_i$

This yields

CPU clock cycles₁ = $2 \times 1 + 1 \times 2 + 2 \times 3 = 10$

CPU clock cycles₂ = $4 \times 1 + 1 \times 2 + 1 \times 3 = 9$

So sequence 2 is faster it takes less clock cycles.

30. (c)

PC-relative $\rightarrow PC + 500 = 202 + 500 = 702$

Base-register $\rightarrow 100 + 500 = 600$